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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/874,239	06/06/2001	Akira Yamada	57454-132	5917

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EXAMINER	
HO, THANG H	

ART UNIT	PAPER NUMBER
2188	7

DATE MAILED: 06/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/874,239	YAMADA, AKIRA	
	Examiner	Art Unit	
	Thang H Ho	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,8-11,13 and 15-20* is/are rejected.

7)☒ Claim(s) *5, 7, 12 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's amendment dated April 12, 2004. The applicant's remarks and amendment were considered with the results that follow.

2. Claims 1-20 are pending in this application for examination. Claims 2, 5-9, 12-14 and 20 have been amended, no claim has been cancelled and no new claim has been added. Therefore, claims 1-20 remain pending in the application.

3. The objection to claims 5-7, 8, 12-14 and 20 is withdrawn due to the Amendment filed on April 12, 2004.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the

reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1-4, 6, 8-11, 13 and 15-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Freerksen et al. (United States Patent 6,557,084), hereinafter Freerksen.

As per claim 1, Freerksen discloses a synchronous signal producing **circuit [FIG. 1, bus controller 128]** for synchronizing access by a processor **[FIG. 1, Processor 120]** and a coprocessor **[FIG. 1, Processor 110]** to a shared memory **[FIG. 1, Main Memory$_{1\text{-}K}$ 130-135, (column 3, lines 61-65)]**, comprising: an access inhibit region register [**a portion of a cache line indicating whether it's in a Modified, Exclusive, Shared, or Invalid state**] for designating an access inhibit region for the processor in the shared memory [**bus controller 128 prevents access to old (i.e., stale or invalid) data from main memory 130 by issuing a signal setting the processor 110 to wait for a time and retry later (i.e., setting processor 110 to a wait state), thereby inhibiting access to the requested region of the main memory until the main memory has been updated**]; a comparing circuit for detecting the access by the processor to the access inhibit region designated in the access inhibit region register [**i.e., compare circuit within bus controller 128 compares the requested data with the data stored in the main memory to determine whether the requested data is invalid**]; and a first logic circuit for issuing a signal setting the processor to a wait state based on a signal indicating that the coprocessor is executing a coprocessor instruction as well as a result of the comparison by the comparing circuit [**logic circuit within bus controller 128 issues a**

signal setting the processor 110 to wait for a time and retry later (column 8, lines 3-26)].

As per claim 2, Freerksen discloses that the first logic circuit issues the signal setting the processor to the wait state based on the signal indicating that the coprocessor is executing the coprocessor instruction, the result of the comparison by the comparing circuit and a signal indicating that locking of the shared memory is to be released **[column 8, lines 3-26]**.

As per claim 3, Freerksen discloses that the synchronous signal producing circuit, further comprising: a bus wait counter for counting the number of bus wait cycles **[column 6, lines 59-62]**; and a second logic circuit for issuing a bus error signal to the processor based on the signal indicating that the coprocessor is executing the coprocessor instruction, the result of the comparison by the comparing circuit and a count value of the bus wait counter **[column 6, line 59 through column 7, line 16]**.

As per claim 4, Freerksen discloses that the synchronous signal producing circuit, further comprising: a first initial value register for setting a wait number at the time when the signal issued by the first logic circuit sets the processor to the wait state; a second initial value register for setting a wait number at the time of normal access by the processor; a selector for selecting the values in the first and second initial value registers based on the signal indicating that the coprocessor is executing the coprocessor

instruction as well as the result of the comparison by the comparing circuit; and a bus wait counter for receiving the value selected by the selector, and issuing a bus error signal to the processor when the bus wait counter counts the selected value **[column 6, line 59 through column 7, line 16]**.

As per claim 6, Freerksen discloses that the synchronous signal producing circuit, further comprising: a coprocessor instruction execution flag for holding information indicating that the coprocessor is executing the coprocessor instruction, wherein the first logic circuit issues a signal for setting the processor to the wait state based on the information held in the coprocessor instruction execution flag and the result of the comparison by the comparing circuit **[column 8, lines 3-26]**.

As per claims 8-11 and 13, the claims encompass the same scope of invention as to that of claims 1-4 and 6, the claims are therefore rejected for the same reasons set forth above with respect to claims 1-4 and 6.

As per claims 15-20, the claims encompass the same scope of invention as to that of claims 1-4 and 6, however the claims are drafted as method format rather than apparatus format, the claims are therefore rejected for the same reasons set forth above with respect to claims 1-4 and 6.

Allowable Subject Matter

6. Claims 5, 7, 12 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record, namely Freerksen, teaches the system and method substantially as claimed. However, the prior art does not teach or suggest a low power consumption mode based on the signal indicating that the coprocessor is executing the coprocessor instruction as well as the result of the comparison by the comparing circuit as recited in dependent claims 5 and 12 and as being argued by Applicant.

Response to Arguments

7. Applicant's arguments filed on April 12, 2004 with respect to claims 1-4, 6-11 and 13-20 have been fully considered but they are not persuasive.

Applicants asserted:

(a) Examiner did not discharge his burden and failed to identify a specific hardware structure as recited in claim 1;

(b) Freerksen does not disclose an "access inhibit register", "comparing circuit" and "first logic circuit" as recited in claim 1;

Examiner respectfully traverses Applicant's remarks for the following reasons:

With respect to (a), firstly, it is unclear which specific hardware structure Applicant is referring to that Examiner failed to identify. Secondly, each hardware structure recited within claim 1 has been fully addressed. For example, a "synchronous signal producing circuit", "processor", "coprocessor" and "shared memory" were

respectively identified as "bus controller 128", "Processor 120", "Processor 110" and "Main Memory$_{1\text{-}K}$ 130-135" as shown in FIG. 1 of the Freerksen reference.

With respect to (b), the cited passage on column 8, lines 3-26 contains an "access inhibit region register", "comparing circuit" and "first logic circuit" as recited in claim 1. Freerksen discloses that bus controller 128 detects and prevents access to old (i.e., stale or invalid) data from main memory 130 utilizing an access inhibit region register (i.e., portion of a cache line indicating whether it's in a Modified, Exclusive, Shared, or Invalid state. Based on detection of stale data being accessed, logic circuit within bus controller 128 issues a signal setting the processor 110 to wait for a time and retry later (i.e., setting processor 110 to a wait state), thereby inhibiting access to the requested region of the main memory until the main memory has been updated. Freerksen also discloses that bus controller 128 detects (i.e., compare circuit within bus controller 128 compares the requested data with the data stored in the main memory) whether the requested data is stale.

Therefore, the rejection of claims 1-4, 6-11 and 13-20 is deemed to be proper. Freerksen's and Yamada's teachings, taken alone or in concert, disclose each and every element recited within claims 1-4, 6-11 and 13-20.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thang H Ho whose telephone number is 703-305-1888. The examiner can normally be reached on Monday-Friday from 7:00 A.M. - 4:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 703-306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thang Ho
Art Unit 2188
June 17, 2004

Mano Padmanabhan 6/18/04

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER